LISTING OF THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1: (currently amended) An apparatus which comprises:

a multi-core processor and

at least one test control mechanism**, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers**;

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said multi-core processor.

2: (original) The apparatus of claim 1, wherein said multi-core processor comprises at least two processor cores and at least one circuit comprising non-processor core logic.

3: (original) The apparatus of claim 2, wherein said multi-core processor and said test control mechanism having a configuration so as to allow testing of at least two processor cores of said multi-core processor.

4: (currently amended) The apparatus of claim 2, ~~wherein said at least one test control mechanism respectively comprises at least one test access port controller (TAPC) and a plurality of distributed data and control registers;~~ wherein said plurality of distributed data and control registers are located both within said at least two processor cores and within said at least one circuit comprising non-core logic.

5: (original) The apparatus of claim 4, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

6: (original) The apparatus of claim 4, wherein said at least one test access port controller (TAPC) is located within said at least two processor cores.

7: (original) The apparatus of claim 4, wherein said at least one test access port controller (TAPC) and at least one of said plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB).

8: (original) The apparatus of claim 4, wherein said distributed test control mechanism is controllable, at least in part, by one of said at least one test access port controller (TAPC).

9: (original) The apparatus of claim 8, wherein which of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is dynamically selectable during operation.

10: (original) The apparatus of claim 2, wherein at least one of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

11: (original) The apparatus of claim 10, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selectable during operation.

12: (original) The apparatus of claim 11, wherein said multiple coupling arrangements are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel and coupling said test access ports for substantially independent operation.

13: (original) The apparatus of claim 10, wherein said at least one test control mechanism is arranged to allow at least one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

14: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow only one of said at least two processor cores' said one test access port (TAP) to be externally visible from said multi-core processor.

15: (original) The apparatus of claim 13, wherein said at least one test control mechanism is arranged to allow the selection of which at least one of said at least two processor cores' said one test access port (TAP) is externally visible from said multi-core processor to occur dynamically.

16: (original) The apparatus of claim 10, wherein said at least one test control mechanism is coupled to produce during operation an error signal if the output signals of said at least two processor cores' said one test access port (TAP) are not substantially equivalent.

17: (original) The apparatus of claim 2, wherein said at least one test control mechanism, said at least one processor core and said at least one circuit comprising non-processor core logic are

further coupled so as to allow testing of said at least one circuit comprising non-processor core logic.

18: (currently amended) A system which comprises:

a computing platform, including:

a memory to store instructions;

a multi-core processor to process instructions which includes:

a plurality of processor cores;

at least one circuit comprising non-processor core logic and

a test control mechanism**, including at least one test access port controller (TAPC) and a plurality of distributed data and control registers**;

said multi-core processor and said test control mechanism having a configuration so as to allow testing of said plurality of processor cores.

19: (original) The system of claim 18, wherein said multi-core processor and said test control mechanism are further arranged so as to allow testing of said at least one circuit comprising non-processor core logic.

20: (currently amended) The system of claim 18, ~~**wherein said test control mechanism comprises at least one test access port controller (TAPC) and a plurality of distributed data and control registers;**~~ wherein said plurality of distributed data and control registers are located both within said plurality of processor cores and within said at least one circuit comprising non-core logic.

21: (original) The system of claim 20, wherein said at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification.

22: (original) The system of claim 20, wherein said at least one test access port controller (TAPC) is located within said plurality of two processor cores.

23: (original) The system of claim 20, wherein said at least one test access port controller (TAPC) and at least one of said a plurality of distributed data and control registers are coupled via an Integrated Test Bus (ITB).

24: (original) The system of claim 20, wherein said distributed test control mechanism is controlled, at least in part, by one of said at least one test access port controller (TAPC).

25: (original) The system of claim 24, wherein which of said at least one test access port controllers (TAPCs) controls said distributed test control mechanism is be dynamically selected during operation.

26: (original) The system of claim 18, wherein each of the said at least two processor cores comprises one test access port (TAP) which includes one test access port controller (TAPC), and a plurality of distributed data and control registers.

27: (original) The system of claim 26, wherein said test control mechanism and said at least two processor cores are coupled so as to provide multiple coupling arrangements, said multiple coupling arrangements being dynamically selected during operation.

28: (original) The system of claim 27, wherein said multiple coupling configurations are selected from a group consisting essentially of coupling said test access ports substantially in series, coupling said test access ports substantially in parallel, and coupling said test access ports for substantially independent operation.

29: (original) The system of claim 26, wherein said test control mechanism is coupled to produce, during operation, a signal that indicates whether the output signals of said at least two processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

30: (original) A method, comprising:

providing an indicator to identify a desired testing option;

based upon said desired testing option, dynamically routing signals between a plurality test access ports (TAPs);

wherein said plurality test access ports (TAPs) are part of a multi-core processor; said multi-processor core including a plurality of processor cores.

31: (original) The method of claim 30, wherein the routing of said signals is selected from a group consisting essentially of coupling said test access ports substantially in series, coupling

said test access ports substantially in parallel, and coupling said test access ports for substantially independent operation.

32: (original) The method of claim 31, wherein providing an indicator to identify a desired testing option comprises storing control information in a register.

33: (original) The method of claim 32, wherein storing control information in a register comprises shifting said data into the register in a serial fashion.

34: (original) The method of claim 32, wherein storing control information in a register comprises a step in compliance with the operation of test data registers as described in the IEEE 1149.1 specification.

35: (original) The method of claim 30, wherein dynamically routing signals between a plurality of test access ports (TAPs) comprises dynamically routing signals between a plurality of test access port controllers (TAPCs) and a plurality of distributed data and control registers.

36: (original) The method of claim 30, wherein dynamically routing signals between a plurality of test access ports (TAPs) comprises only altering the routing of signals external to said plurality of processor cores.

37: (original) The method of claim 30, which further comprises producing a signal that indicates whether the output signals of said at least two processor cores' said one test access port (TAP) are equivalent or substantially equivalent.